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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/858,400	05/16/2001	Eric Gerritsen	97-CCP-251 DIV	2138

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EXAMINER	
NGUYEN, THANH T	
ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 09/26/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/858,400	GERRITSEN ET AL.	
	Examiner	Art Unit	
	Thanh T. Nguyen	2813	

-- The MAILING DATE of this communication appears on the cov r sheet with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21 and 30-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21 and 30-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1-21, 30-35 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-21, 30-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwata et al. (U.S. Patent No. 6,255,702) as applied to claims 1-10, 12-19, and 21 above.

Referring to figures 14a-14c, 15d-15f, 16g-16i, 17j-17k, teaches a method for forming a low resistivity titanium silicide layer on a surface of a doped region of a silicon semiconductor substrate, the method comprising the steps of:

Depositing a titanium layer (416, see fig. 16h, col. 30, lines 11-13) on the surface of the doped region (409, Indium, see figure 14d, col. 29, lines 40-45) of the silicon semiconductor

substrate (401, see figure 14a, col. 29, lines 13-15), the doped region being an n-type or p-type source or drain region (415);

Introducing an effective amount of a metallic element at least at the interface between the titanium layer (416) and the doped region (401) of the silicon semiconductor substrate (401) so as to promote titanium silicide transformation from C49 phase to C54 phase during a subsequent rapid thermal annealing, the metallic element being chosen from the group consisting of indium, gallium, tin, and lead, and

After the introducing step, performing a rapid thermal annealing of a titanium-coated silicon semiconductor substrate (see figure 16i, col. 30, lines 47-65) to from titanium silicide (418).

Regarding to claims 2, 3 and 16, the metallic element is chosen from the group consisting of indium (see figure 14d, col. 29, lines 40-45).

Regarding to claims 4-6 and 17, the effective amount of the metallic element is $1x10^{13}$-$5x10^{14}$ atoms/cm^2 (see figure 14d, col. 29, lines 45-49).

Regarding to claims 7 and 18, the introducing step includes the sub-step of depositing the effective amount of the metallic element on the surface of the at least one doped area of the silicon semiconductor substrate (see figure 14d, col. 29, lines 40-50).

Regarding to claims 8 and 19, the introducing step includes the sub-step of implanting the effective amount of the metallic element on the surface of the at least one doped area of the silicon semiconductor substrate (see figure 14d, col. 29, lines 40-50).

Regarding to claims 9 and 14, implanting the sub-step is performed before the depositing step (see figure 14d, col. 29, lines 40-50).

Regarding to claims 12-13 and 21, implanting sub-step, the implantation energy is approximately 25 keV (see figure 14d, col. 29, lines 40-50).

Iwata et al. teaches all of the limitation that described in the claimed invention above. However, the reference does not teach the specific depth of the implanted region (in claims 11 and 20).

The specific depth of the implanted region are considered to involve routine optimization while has been held to be within the level of ordinary skill in the art. As noted in *In re Aller 105 USPQ233, 255 (CCPA 1955),* the selection of reaction parameters such as temperature and concentration would have been obvious:

> "Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art...such ranges are termed "critical ranges and the applicant has the burden of proving such criticality.... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation."
> *In re Aller 105 USPQ233, 255 (CCPA 1955). See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).*

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time the invention was made would have used any depth range suitable to the method in process of Iwata et al. in order to optimize the process.

Response to Arguments

Applicant's arguments with respect to claims 1-21, 30-35 have been considered but are moot in view of the new ground(s) of rejection.

Applicant contends that Iwata does not disclose a method in which a titanium layer is deposited on the surface of an n-type or p-type doped region of silicon semiconductor substrate, an effective amount of indium, gallium, tin or lead is introduced at the interface between the titanium layer and the doped region of the silicon semiconductor substrata so as to promote titanium silicide transformation form C49 phase to C54 phase during a subsequent rapid thermal annealing, and a rapid thermal annealing is performed so as to form titanium silicide. In response to applicant that Iwata does disclose a method in which a titanium layer (416) is deposited on the surface of an n-type or p-type doped region (409, Indium, see figure 14d, col. 29, lines 40-45) of the silicon semiconductor substrate (401, see figure 14a, col. 29, lines 13-15), the doped region (415) being an n-type or p-type source or drain region (415); an effective amount of indium, gallium, tin or lead is introduced at the interface between the titanium layer (416) and the doped region (415) of the silicon semiconductor substrate (401) so as to promote titanium silicide transformation form C49 phase to C54 phase during a subsequent rapid thermal annealing, and a rapid thermal annealing is performed so as to form titanium silicide (417/418, see figure 16i, col. 30, lines 47-67, col. 31, lines 1-17). Since the annealing step to form the titanium silicide transformation form C49 phase to C54 phase during a subsequent rapid thermal annealing. Which means that the annealing step is occurring, or carried out at a time after the introducing the metallic element.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (703) 308-9439, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:30AM to 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached on (703) 308-4940. The fax phone number for this Group is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956 (**See MPEP 203.08**).

Thanh Nguyen
Patent Examiner
Patent Examining Group 2800

TTN
September 22, 2003